VERY HIGH EFFICIENCY TECHNIQUES AND THEIR SELECTIVE APPLICATION TO THE DESIGN OF A 70A RECTIFIER

DES TECHNIQUES HAUTEMENT EFFICACES ET LEUR APPLICATION SELECTIVE A LA CONCEPTION D'UN REDRESSEUR DE 70A

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Résumé

Les toutes dernières techniques utilsées dans la conception et la construction de blocs d'alimentation à commutateur d'une efficacité et d'une performance élevées sont étudiées, comparées à des techniques plus anciennes, et mises en oeuvre dans la conception optimisée d'un redresseur télécommunications de 70A, 54V en continu, dont le facteur de puissance unité est dérivé de l'alimentation secteur, avec un taux d'efficacité dépassant 93%. On a introduit un nouveau limitateur (amortisseur) 'sans perte', qui combine les propriétés de limitation $\delta i/\delta t$ et $\delta v/\delta t$, afin d'améliorer sensiblement l'efficacité tout en utilisant 30% moins de pièces que les limitateurs classiques 'à forte perte'. Une autre innovation a été l'utilisation parallèle d'IGBT et de MOSFET en vue de créer un commutateur marche-arrêt hybride subissant une très faible perte lors de la mise sous tension et une faible perte lors de la mise hors tension. Contrairment à la tendance générale, la fréquence de commutation a été réduite pour minimiser tes pertes de commutation. La combinaison de ces techniques, et d'autres dont on discute dans l'article, donne d'excellents résultats du point de vue de l'efficacité, sans parler de certains avantages réels, quoique non évidents, dont profiteront tant le fabricantque l'utilisateur final.

Abstract

Latest techniques for the design and construction of high efficiency, high performance switched mode power supplies are investigated, compared with older techniques, and implemented in the optimised design of a 70A, 54VDC telecommunications rectifier which draws unity power factor from the AC supply while exceeding 93% conversion efficiency. A new lossless' snubber is introduced which combines di/dt and dv/dt limiting properties to greatly improve efficiency while using 30% fewer parts than conventional 'lossy' snubbers. Another novel approach used is the parallel combination of IGBT and MOSFET to form a hybrid power switch with a very low on-voltage and a low turn-off loss. Contrary to popular trends the switching frequency is kept low to minimise switching losses. The combination of these techniques and others discussed in the paper, yields a unit with excellent efficiency and some non-obvious advantages which further benefit both manufacturer and end user.

Introduction

The task of designing a superior rectifier for telecommunications use has prompted an investigation into new devices and techniques with an emphasis on achieving an overall optimum result. This process of optimisation involved balancing the cost, size, weight, reliability, serviceability, and manufactureability of the design while meeting all electrical performance requirements. Such an approach led to the first design goal - maximising efficiency. As efficiency improves less heatsink (component cooling) area is required thus reducing the product's size and weight. In addition end users prefer high efficiency since it saves electricity costs and relieves air-conditioning requirements. All factors in the optimisation are adversely effected by circuit complexity, which led to the second design goal, that the power circuit topology be simple and be able to be controlled in a straightforward manner.

The rectifier was to deliver 70A at 54V while drawing sinusoidal current from a nominal 240VAC supply (180-275V range), achieve 92% or higher efficiency over a wide range of load conditions (representing 20% less loss than industry standard products), be low cost and uncomplicated.

The size of heatsink required for natural convection cooling of the rectifier (assuming the efficiency goal was achieved) was such that the size of the magnetic components needed to operate at frequencies as low as 25kHz would not greatly increase the overall size of the unit. Also the efficiency of the switching devices would be enhanced the lower the frequency, regardless of the type of converter. These factors led to the expectation that a rectifier operating at a low switching frequency would be optimum for this application.

Topology

Requirement

The requirement was that the topology best utilise the semiconductor and passive elements, be simple and controllable, whilst being able to meet all electrical performance needs. A typical rectifier topology consists of an AC-DC converter (usually a diode

bridge), a power factor correction stage, an energy storage element to supply energy during the zero crossings of the input voltage, an isolating stage, and a DC-DC converter to finely regulate the output (usually these last two are incorporated in one stage) as shown in Fig 1.

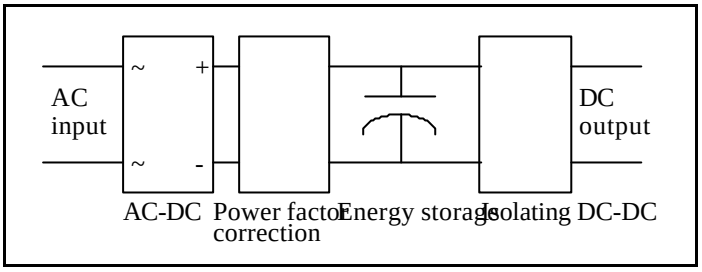

Fig 1. Block diagram of rectifier

Power factor correction stage

In order to provide power factor correction in a single phase application a converter must be able to draw controlled current as the input voltage approaches zero. Eligible converters are the Boost, Buck-boost, Sepic, Zeta, and Cuk varieties. Of these all except the Boost can have their output voltage lower or higher than the input which gives them both an advantage and a cost in this application. Their advantage is their ability to 'soft start' the energy storage capacitor when AC power is first applied. Soft starting is necessary to prevent current and voltage spikes being applied to the AC supply, to prevent excessive wear on switches or circuit breakers controlling the supply, and to allow operation with standby power systems such as motor generator (MG) sets. The disadvantage of these converters is the high voltage and current requirement placed on the semiconductor switch. The Boost converter must be used with some auxiliary means of soft starting such as a series resistor / relay combination but the advantages gained in the switch requirement outweigh this difficulty - Table 1.

	Boost stage, 280VAC in, 440VDC out, 9A average out	Buck-Boost, sepic zeta, or cuk; same conditions
Maximum switch V	440V	840V
Maximum diode V	440V	840V
Peak switch current	20A	20A
Peak diode current	20A	20A
Average switch I	less than 10A	14A
Average diode I	9A	9A

Table 1. Semiconductor stress comparison

The Boost converter has additional advantages - it uses the minimum number of passive elements, is easy to control, and draws non-pulsating (trapezoidal) current from the AC supply which makes the task of filtering relatively easy.

Isolating DC-DC conversion stage

The differences in switch requirements are less dramatic in DC-DC converters than in the above case and the following factors assume greater importance:-

Clamping: The ability to transfer the energy stored in the leakage inductance of the transformer to the energy storage capacitor at turn-off, eliminates the requirement for lossy passive clamps which would be required to limit the peak voltage across the switch or switches. The clamping requirement rules out most of the single ended converters and the Push-pull converter. Those with auxiliary clamp windings divert most of the leakage current to the energy storage capacitor, but never all of it due to the leakage inductance between the clamp winding and the other primary winding.

Capacitor size: High voltage electrolytic capacitors generally have a higher volumetric efficiency than low voltage ones. Referring to Fig 2, a power supply of 500VA at 250V delivers 2ADC and a typical 250V capacitor smoothing that supply has a ripple rating of 2.5A. If the voltage of the supply was 50V, 10ADC would be delivered but the same sized 50V capacitor smoothing it has a ripple rating of only 4.6A. Clearly any high ripple site in the topology should be at a high voltage if the smallest capacitor is to be used. Consequently the DC-DC conversion stage should draw pulsating (high ripple) current from the energy storage capacitors which must be large anyway, and deliver non-pulsating (trapezoidal) current to the output so that small capacitors can be used there.

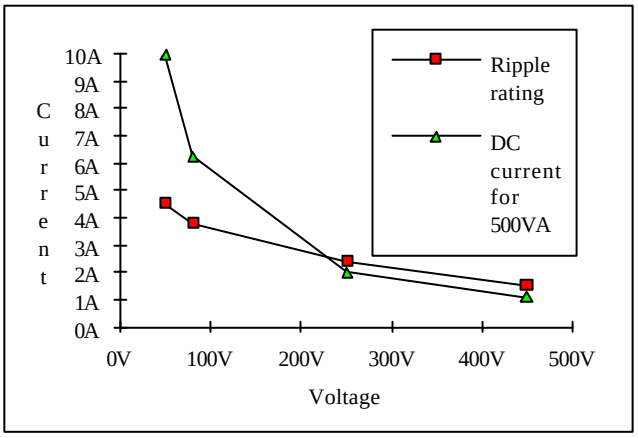

Fig 2. Ripple rating vs. voltage rating for capacitors of the same

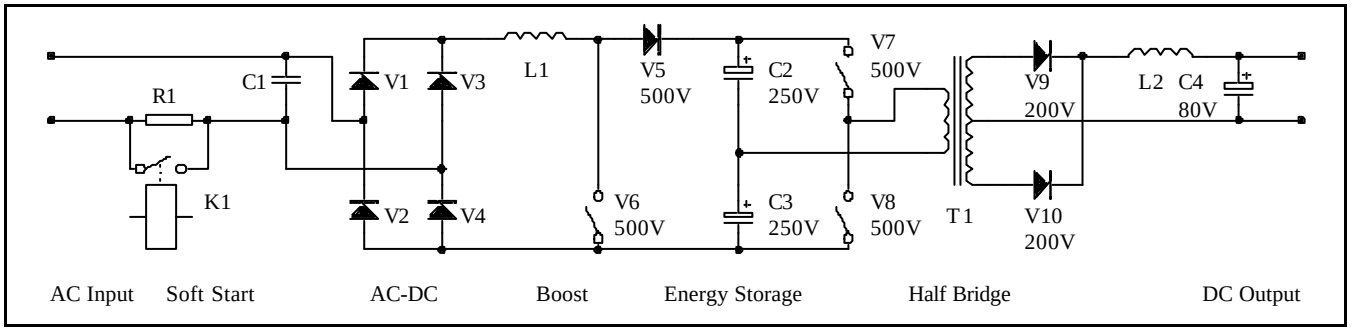

Fig 3. Chosen circuit topology

physical size [1]*, and the DC current required to deliver 500VA at these voltages.*

Output choke size: The size of the output choke required to deliver non-pulsating current to the output capacitors decreases as ripple frequency and duty cycle increase. 'Symmetrical' converters which combine alternating pulses of equal size in the secondary have a duty cycle approaching 100% when delivering maximum output voltage, whereas a well-designed 'asymmetrical' converter has a duty cycle of around 50% under the same conditions, thus symmetrical converters are more desirable. In addition the symmetrical converter's output ripple frequency is twice that of its switches, further reducing output choke size.

Isolation transformer size: Symmetrical excitation of a transformer of a given size generally achieves the greatest throughput due to the maximum use being made of its allowable peak to peak flux excursion. At low frequencies the increase in throughput is at least 50% [2].

Topologies which are suitable after considering the above factors are the Full-bridge and Half-bridge converters with current fed outputs. The Half-bridge has the advantage of requiring only two switches and has a more favourable turns ratio in the isolation transformer which allows more throughput. Its main disadvantage is its requirement for capacitive coupling to the DC supply in the primary, but this can be provided by splitting the energy storage capacitors. Referring to Fig 2, 250V capacitors perform nearly as well as 450V ones in terms of their ripple current to voltage ratio, and usually cost much less, so it was concluded that the slight capacitor size penalty incurred by the Half-bridge was made up for by the gains in simplicity, cost and transformer throughput. The optimum topology is shown in Fig 3.

Switching devices

The topology of choice requires three switches, with a voltage rating of at least 500V, and with the capability of switching at least 40A peak and conducting 20A rms in order to cope with the extremes of operation.

Bipolar Transistors

Large bipolar transistors generally have switching speeds which are too slow for them to be attractive in converters operating above 20kHz. In addition to a slow fall time they are slow to turn on and have a long delay before turning off (storage time) which limits their controllability. Some small bipolar transistors are sufficiently fast to be considered but have insufficient current handling for this power level without paralleling multiple devices (difficult - current hogging). Bipolar transistors do have a low on-voltage but require a continuous and large base current while on which diminishes this benefit. Reverse bias safe operating area restrictions force the use of large snubber networks.

GTOs, ASCRs

These devices require severe snubber or resonating networks and are becoming difficult to obtain since most manufacturers are contracting or deleting their offering.

MOSFETs

MOSFETs are near ideal switches having very fast rise and fall times, short effective storage times, excellent safe operating area, and simple drive requirements. There is no built in voltage in the conduction path but only a series resistance which modulates between a very high value when the device is off and a minimum value when on. Unfortunately 500V devices have a high on-resistance per unit die area which makes their effective on-voltage high. Paralleling is relatively easy so the on-resistance (and on-voltage) can be reduced to any value at the cost of additional devices and complexity. The on-resistance typically doubles from 25^{o}C to 130^{o}C which makes conduction loss very temperature sensitive and leads to the possibility of thermal runaway. Paralleling of large numbers of devices increases turn-on loss due to the discharge of the output capacitance of each device in circuits which do not exhibit ZVS (zero voltage switching) behaviour, and increases gate drive power loss in all circuits.

IGBTs

These devices behave like a combination MOSFET and bipolar transistor having the MOSFET's easy drive requirement, excellent safe operating area, and fast turn-on, as well as the bipolar's low on-voltage. However they have the problem of a high turn-off switching loss due to the well know "tail" current which limits their advantage in hard switched circuits operating above 20kHz.

Summary

Of the devices considered IGBTs offer the most potential for high efficiency because of their low conduction losses and ease of use, but some means of limiting their turn-off loss is required to fully utilise their benefit.

Switching Techniques for IGBTs

IGBTs are available in at least two different versions from most manufacturers - a low turn-off loss version with a relatively high on-voltage, and a low on-voltage version with a relatively high turn-off loss [3],[4]. A switching technique which could accommodate either version of IGBT was desired to increase the choice of applicable devices and hence improve availability and lower cost.

The two most common techniques which are currently being utilised to overcome IGBT turn-off loss problems are as follows:

Zero Current Switching

This requires a resonant approach in which, at turn-off, the current through the IGBT reverses and flows through an antiparallel diode for a sufficient time for the tail current to decay to a small value, after which the voltage becomes positive across the IGBT. Resonant, quasi-resonant and quasi-squarewave converters all achieve the same result, as do any converters suitable for SCRs. Both IGBT versions can be used if the appropriate current reversal time is applied. The principal disadvantages are:

i) an extra parallel diode with high current rating is required across each switch to conduct the reverse resonating current.

ii) the conducted RMS current is considerably higher than that of a PWM stage because of the resonant circuit, thus the conduction loss in the IGBT and any other components that this current flows through increases.

iii) the peak current is typically twice that of a PWM stage operating at maximum output, and it does not decrease much when the output power decreases. Although IGBTs handle high peak currents well, their on-voltage does increase resulting in a larger loss.

iv) in many ZCS implementations, the output diode voltage rating needs to be a factor of 2 higher than that for PWM stage, which results in a consequently higher forward on-voltage - e.g. 0.8 volts for 200V diodes versus 1.2 volts for 400V diodes. This translates into an extra 30 watts loss at 70A (almost 1% worse efficiency).

v) in a typical ZCS circuit, efficiency at load currents of 50 - 80% of maximum is significantly lower than at its full output current rating because of the high and near-constant circulating current. However, in rectifier/battery charger applications for which this unit is designed, it is highly desirable for the best efficiency to be achieved at currents less than the maximum rating, as the rectifier operates in this mode, with batteries fully charged, for typically more than 99% of its life!

Note: Auxiliary commutated ZCS where an auxiliary switch injects a reversing current into the main switch and is itself ZCS, achieves theoretically a conduction loss much closer to PWM. The minimum duty cycle available to this scheme is restricted by the commutation time of around 1.5*u*sec required by each IGBT (3*u*sec total), and the peak current is still twice that of PWM. To implement such a scheme requires two IGBTs, two antiparallel diodes, a resonating network, and a complex control circuit for each 'switch' so it was not considered on grounds of being overly complex.

Large dv/dt Snubber Capacitor - Zero Voltage Switching

A capacitor to limit and reduce the rate of rise of voltage after switch-off can be added to an IGBT as part of a passive or lossless snubber circuit [5]. Zero Voltage Switching topologies including the phase shifted full bridge achieve the same result - i.e. ensure a slowly rising voltage on the IGBT so that while the "tail" current is large the voltage across the device is small. A reduction in the switch-off power of up to 3:1 can be achieved in this manner for most IGBT types with rise times of around 4*u*sec. Clearly the low turn-off loss devices are most suitable for this technique.

A greater reduction was needed because the total power loss - conduction plus switching loss - was still too high (using the lowest turn-off loss device available) for a single TO-247 device to be used at the worst case conditions of high temperature and low AC mains voltage.

Parallel IGBT/MOSFET Combination

It became clear that the combination of the low conduction loss of the IGBT with the low turn-off loss of the MOSFET is highly desirable. This combination can be achieved by paralleling the devices and staggering the timing of their gate drives. This approach permits the use of normal PWM techniques while achieving low loss, and is applicable to both versions of IGBT.

Extensive tests indicated that the "tail" current shape does not change significantly if the voltage across the IGBT during turn-off is a few volts or hundreds of volts. Thus by turning off the IGBT in parallel with the MOSFET between 1 and 1.5 *u*sec before turning off the MOSFET - see Fig 4, the current is "carried" by the MOSFET during the last 1.5*u*sec while the IGBT junctions recover as shown in Fig 5.

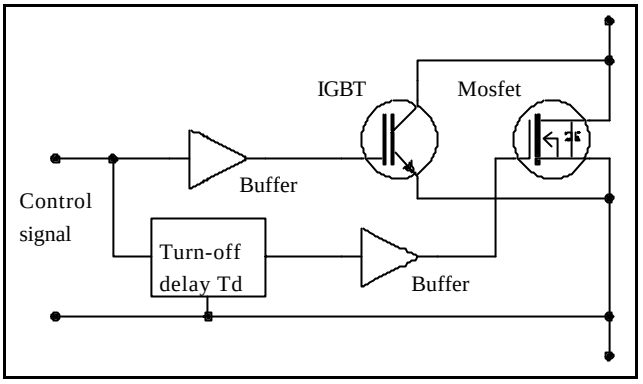

Fig 4. Schematic of the hybrid switch

Using this approach, the combined switching-off loss can be made equivalent to that of a MOSFET stage, yet this combined conduction loss could only be achieved by using 4 or 5 times more MOSFETs in parallel. As an example, with the industry standard IRFP460 switching 35 amps (as required in the Boost stage of this unit) at a junction temp of 140^{O}C (worst case, 50^{O}C ambient) the on-voltage would be close to 18 volts. This compares with around 2 volts for a typical 600V, 50A "Fast" IGBT at the same temperature - a very considerable benefit!

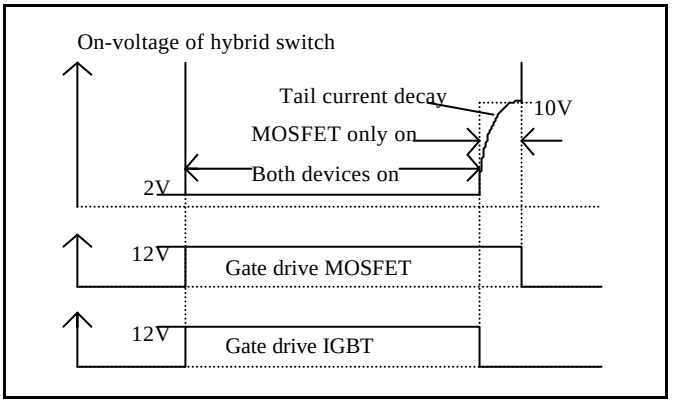

Fig 5. Idealised waveforms of the hybrid switch

The trigger delay circuit is designed to have a constant delay for on-times above 2 *u*sec. At on-times below 2 *u*sec, the delay is progressively reduced to be zero at zero on-time. This characteristic is necessary to cope with short circuit conditions, during which time the required duty cycle in the Half-bridge can be well below 2*u*sec. Similarly, in the Boost stage, the duty cycle regularly drops toward zero at the AC voltage cross-over. In both instances the switch-off loss is less than optimum under those conditions (a significant amount of the tail current is still present), but since the conduction loss is greatly reduced when the on-time is near zero, an increase in turn-off loss is tolerable.

Example:

At switch-off, the Half-bridge power switches must contend with 28 A peak and 440 VDC.

The typical turn-off energy quoted for an IRGPC50F type IGBT is approximately 7mJ at the maximum expected junction temperature (140^{o}C) and approximately 3.5mJ for junction temperatures at around 40^{o}C corresponding to more normal operating conditions.

There are two components of switch-off loss when a MOSFET is used to implement the switch-off.

i) Conduction loss given by Ec = I^2 x Rdson x Td where Td is time for which MOSFET is held on after IGBT is turned off (1.5*u*sec). An IRFP460 type MOSFET has a typical Rdson (on-resistance) of 0.26 ohm at 40^{o}C and 0.53 ohm at 140^{o}C. Thus Ec = 0.31mJ at low temperature and 0.62mJ at high temperature.

ii) Switch-off loss - this term is more difficult to calculate due to effect of the parallel RC EMI snubber and through not knowing the exact current voltage relationship. The best estimate from calculations and switching tests is 0.1 mJ at both low and high temperatures.

It can thus be seen that the turn-off loss is reduced by up to a factor of 10 at high or low temperatures by using a MOSFET to effect the turn-off. The delay of 1.5 *u*sec is believed to be sufficiently long to allow sufficient recovery of the IGBT "tail" even at the highest expected temperatures.

From the above figures, the turn-off loss at low temperatures is expected to be approximately 10 watts (0.41 mJ x 25kHz) for each of the 2 MOSFETs in the Half-bridge.

The total loss measured in the MOSFET would be expected to be different due to three other factors:

a) Turn-on loss in the MOSFET (which is shared by the IGBT) which is only a few watts in total due to the slowly rising primary current (limited by the leakage inductance).

b) Since the MOSFET is on during the total conduction time of approximately 18*u*sec, it will carry some of the conduction current which in the case of the IRFP460 amounts to approximately 4 watts loss. It should be noted that the loss component decreases as the junction temperature (and therefore Rdson) increases.

c) There is a compensating factor which is due to the fact that current in the MOSFET is not 28A during the entire 1.5*u*sec as the IGBT initially carries significant current with its characteristic tail - Figs 5 and 11.

Taking all these factors into consideration, the total loss for the MOSFETs will be around 10 watts at low temperatures. This is not far off the figures obtained by calorimetric measurements and shown in Table 2.

Switching frequency

As described above, the turn-off loss for the parallel IGBT / MOSFET combination is low but not zero. The turn-off losses are proportional to frequency as is the turn-on loss. At 25kHz total switching losses are about 40% of conduction losses; at 50kHz they increase to 80% etc. There is a clear efficiency benefit in operating at the lowest possible frequency from the switching loss viewpoint and as suggested previously there is little detriment to the size and weight of the complete unit due to the larger magnetic components required. An operating frequency of 25kHz was chosen to allow a guard band from the audio range (20kHz and below).

New Lossless Snubber

Reasons for requiring a snubber:

i) Reduce maximum power dissipation per power semiconductor package (TO-247) to less than 20 watts each worst case. This would allow the use of a shield on each power switch to suppress EMI without compromising the lifetime or reliability of the semiconductors.

ii) Reduce the di/dt and dv/dt to controlled levels for lower EMI currents and fewer problems with control circuits disturbed by interference noise.

iii) Reduce peak-power induced thermal stress in the power semiconductors which further improves long-term reliability.

Examination of the two power stages lead to the conclusion that the Boost stage, with its high voltage diode's reverse recovery giving rise to high turn-on power in the switch and its inductive turn-off making the switch-off power significant, would benefit most from the application of snubber circuitry. The Half-bridge already has di/dt limiting built in by the transformer's leakage inductance, thus the reverse recovery of the output diodes does not result in a significant turn-on loss in the switches.

The reluctance to add the conventional di/dt and dv/dt passive snubbers to the Boost stage was due to the addition of the extra components. As well, the overall power loss would not be decreased by these snubbers.

Lossless snubbers were considered but were, at first, off-putting due to the further increase in added components [6],[7].

Finally, however, a combined di/dt and dv/dt snubber circuit was evolved, for which a patent has been applied, which has zero current turn-on and zero voltage turn-off properties, and achieves all of the objectives with a minimal number of components. The circuit is shown incorporated into a Boost stage in Fig. 6 and the associated principal waveforms are shown in Fig. 7. The snubber components are L1, C1, C2, D1, D2 and D3.

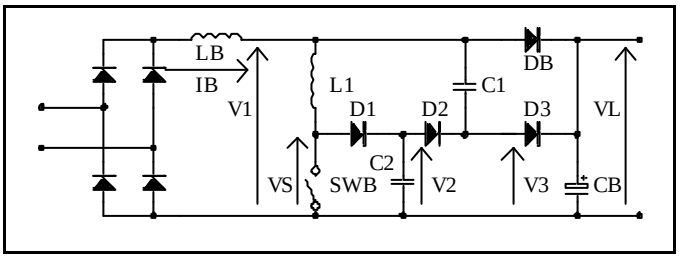

Fig 6. Boost circuit incorporating the new snubber.

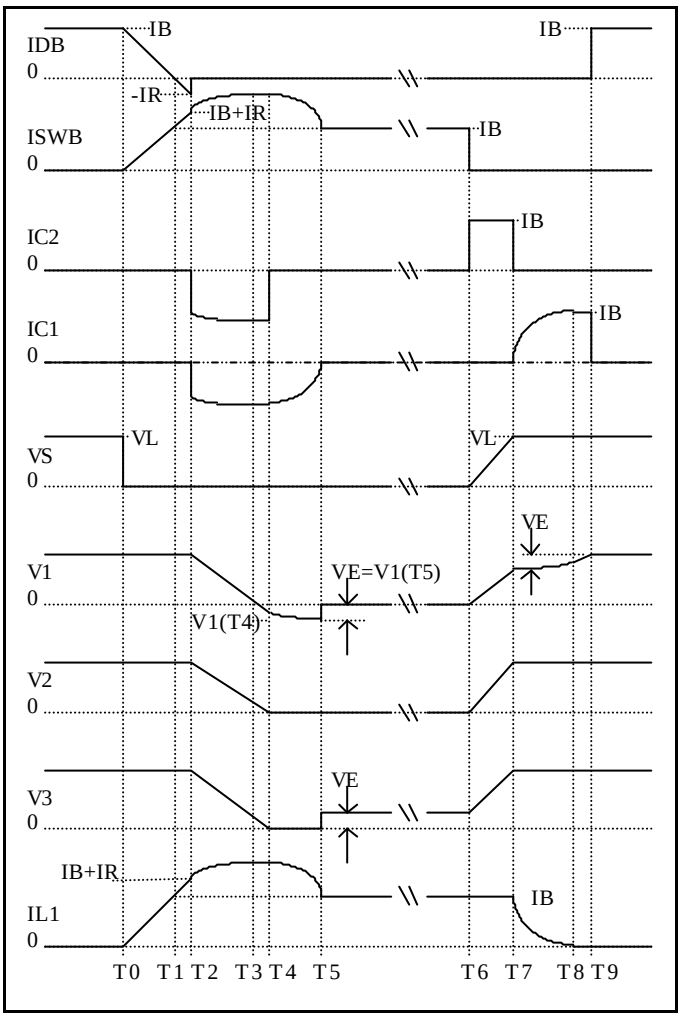

Fig. 7 shows the various waveforms at different parts of a switching cycle.

The starting point is with current I_B flowing through D_B to the load. The current through L_1, D_1, D_2, D_3 and SW_B is zero as is the voltage across C_1. The voltage V_2 on C_2 is approximately equal to V_L. It is further assumed that $C_1 >> C_2$; e.g. $C_1 = 10\ C_2$.

At T_0, SW_B turns on and the current through it increases from zero at a controlled rate given by:

$$\frac{\partial I_{L1}(T0)}{\partial t} = \frac{V_L}{L_1} \qquad (1)$$

Since the voltage across SW_B falls rapidly to zero, its turn-on power loss is low.

The current through D_B will linearly fall to zero at time T_1 and continue to decrease until reverse recovery current I_R flows at T_2.

At T_2 D_B turns off, D2 turns on, and voltages V_1, V_2 and V_3 begin to fall thus beginning the discharge of C_2 towards zero volts.

The current causing C_2 to discharge is equal to the difference between I_B and I_{L1} which equals the reverse recovery current I_R to begin with, but in the time period T_2 to T_3, it increases to a higher value due to the increase in current through L_1 caused by the positive voltage V_1 applied to it. At T_3, V_1 is zero volts but because of the charge attained by C_1 in this period (charge taken from C2 via D2), the voltages V_2 and V_3 are positive.

From T_3 to T_4 the voltage across L_1 becomes negative, so the current through it begins to decrease. However, the net current flowing through C_2 and C_1 is still equal to the difference between I_B and I_{L1}.

At T_4 the voltage on C_2 (V_2) is just less than zero and all the energy stored in C2 has been transferred to C1 via D2. Hence:

$$V_{1(T4)} = -V_L\sqrt{\frac{C2}{C1}} \qquad (2)$$

At T_4 D_1 begins to conduct, thus clamping V_2 and V3 to approximately zero volts (ignoring SW_B forward voltage and D_1, D_2 voltage drops).

Between T_4 and T_5, a resonant ¼ cycle ring occurs during which the excess energy stored in L_1 due to both the reverse recovery of D_B and the discharge of C_2, is transferred to C_1 so that the voltage V_1 is given by:

$$V_{1(T5)} = \sqrt{\frac{C2V_L^2}{C1} + \frac{L1(I_R^2 + 2I_RI_B)}{C1}} \equiv V_E \qquad (3)$$

By inspection, it can be seen that even if I_R = 0, V_E ($V_{1(T5)}$) will still have a positive and finite value due to the energy transferred by C2, ensuring a "resetting" of L_1 during the turn-off phase.

At T5 the current IL1 equals IB, current stops flowing into C1 via D1 and D2, the voltage across L1 collapses thus V1 increases from -VE to 0V, and V3 rises from 0V to +VE. V2 stays at 0V because D2 is reverse biased.

When SW_B is turned off at T_6, the current I_B flowing through L_1 will flow through D_1 and C_2 thus causing the voltage across SW_B to increase from zero at a rate given by:

$$\frac{\partial V_S(T6)}{\partial t} = \frac{I_B}{C_2} \qquad (4)$$

Since the current in SW_B falls rapidly to zero, its turn-off power loss is low.

At T_7, D_2 and D_3 also become forward biased and clamp the switch voltage and C_2 voltage to V_L, the output voltage. At this point, current begins to flow in the loop formed by L_1, D_1, D_2 and C_1, and current in C_2 drops to zero. The voltage across L_1 at this time is -V_E so current in it begins to drop from its value I_B. The increasing difference current between I_B and the current through L_1 flows out of C_1 and begins to discharge it as shown in Fig 7 between T_7 and T_8.

At T_8, D_1 and D_2 turn off and L_1 is fully reset with current through it being zero. If the voltage across C_1 is still not zero, the current I_B through C_1, D_3 will continue the discharge of C_1 until at T_9 its voltage is zero and D_B is thenceforth forward biased and conducts current I_B. At this point L_1 and C_1 are reset and the circuit is ready for a new cycle.

Some of the significant features of the circuit are:-

1. The maximum voltage of SW_B is V_L, the output voltage.

2. The maximum reverse voltage on D_B, the main Boost diode, is $V_L + V_E$ and is well defined by the relative values of I_R, L_1, C_1 and C_2.

3. The maximum rate of rise of current through SW_B is well defined by L_1 and V_L and its turn-on loss and stress is low.

4. The maximum rate of rise of voltage across SW_B is well defined by C_2 and the turn-off power loss and stress is low.

5. The energy stored in L_1 and C_2 during the switching cycle in order to achieve control of the rate of rise of current and voltage is returned to the output supply thus ensuring a substantially lossless operation.

It is worth noting that if C2 is removed and D2 is short circuited then the circuit provides di/dt limiting only, and thus becomes a 'lossless' di/dt snubber.

In Fig. 8 several components are added to the circuit shown in Fig. 6 in order to improve non-ideal behaviour.

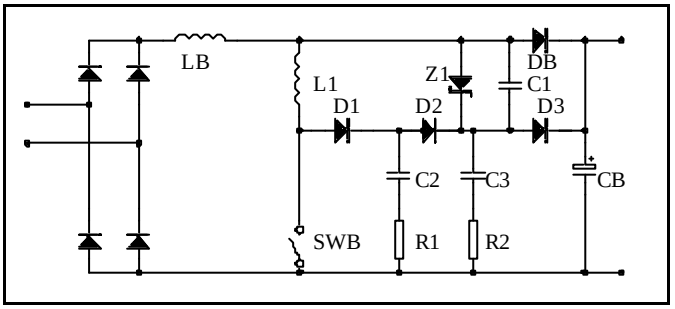

Fig 8. Circuit of Fig 6 with enhancements to new snubber.

R_1 is added to dampen resonant oscillations which would otherwise occur at times T_4 and T_7. R_2 and C_3 are added to dampen oscillations which occur at times T_2 and T_5. Z_1 is a zener diode which prevents excessive voltage build-up on C_1 when current in L_B becomes discontinuous at light loads. The combined power dissipation of R1, R2, and Z1 was less than 1W at full power so the 'lossless' nature of the snubber is preserved.

Overall results

The efficiency and power loss results shown in Figs 9 and 10 were obtained from our prototype with all EMI filtering measures installed but no allowance made for the loss in the connectors which were not finalised at the time of writing. A Voltec PM-3000A power analyser was used to measure input power, and +/- 0.05% accuracy multimeters measured output volts and the voltage across a calibrated shunt giving a total measurement uncertainty of +/- 0.2%.

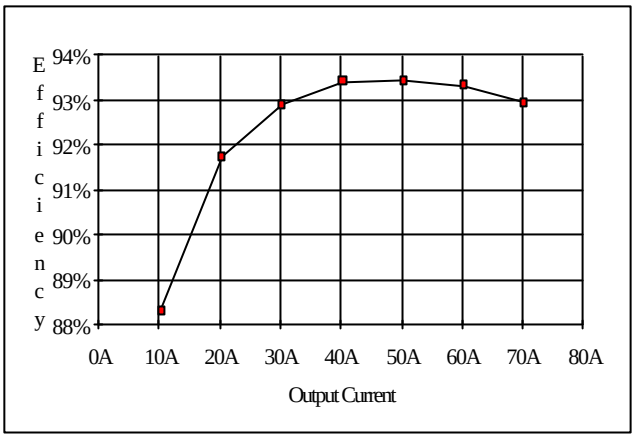

Fig 9. Efficiency verses output current at 54VDC out, 240VAC in.

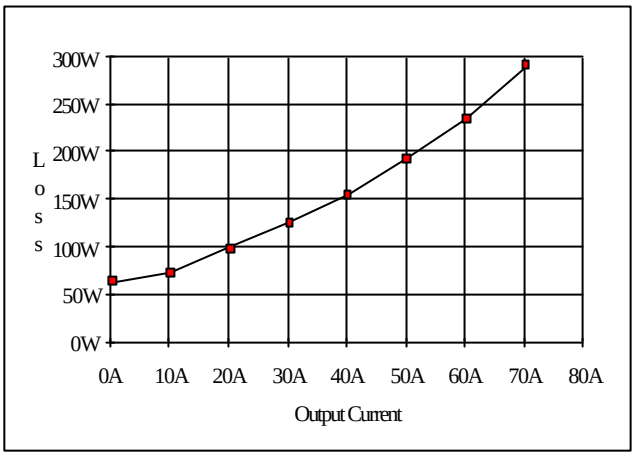

Fig 10 Power loss verses output current at 54V out, 240VAC in.

Table 2 shows the result achieved in the Half-bridge. Note the well balanced distribution of loss between the two devices. As the devices heat the total loss increases but at a low rate; at 100^{o}C total loss increased by 4W or 22% which compares favourably to the temperature sensitivity of other switching schemes. This result was attained by heating the switching devices separately and observing the increase in input power.

P_{IGBT}	P_{MOSFET}	P_{total}
9.5W	9.0W	18.5W

Table 2: Power loss of the hybrid switch in the Half-bridge stage. Conditions: 440VDC in, 54VDC out, 70ADC out, 25^{o}C. Components: IGBT=IRGPC50F, MOSFET=IRFP460.

Table 3 shows the effect of the new snubber on the Boost stage. Note that without the snubber the loss in the MOSFET is so high that at high ambient temperature the device's reliability would be compromised. The effect of the snubber is to reduce the total power loss to 63% of the hard switched value.

	P_{IGBT}	P_{MOSFET}	$P_{snubber}$	P_{diode}	P_{total}
No snubber	15.1W	20.3W	Nil	10.8 W	46.2W
New snub.	6.8W	8.2W	~ 4W	9.9W	28.9W

Table 3: Power loss of the hybrid switch and diode in the Boost stage with and without the new snubber. Conditions: 220VAC in, 440VDC out, 4kW out, 25^{o}C. Components: C1=200nF, C2=4.7nF,

L1=1.8uH, IGBT=APT55GF60BN, MOSFET=IRFP460, Diode=DSEI60-06A.

Fig 11 shows the actual oscilloscope waveforms of the hybrid switch during turn-off. The turn-off 'tail' of the IGBT is clearly visible and the behaviour is close to the idealised behaviour shown in Fig 5.

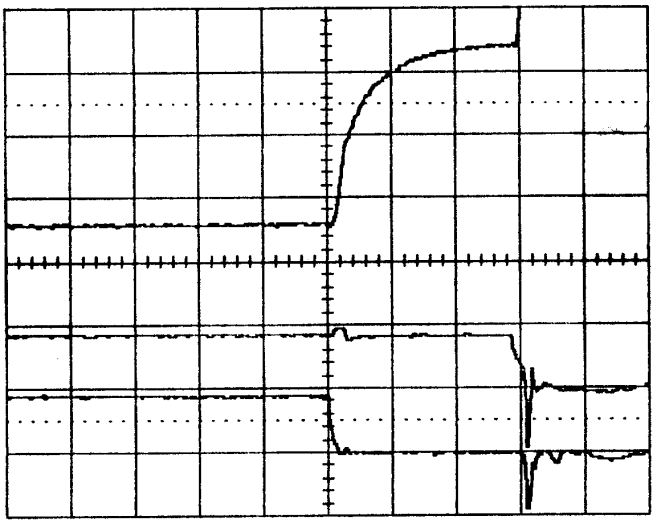

Fig 11. Observed hybrid switch performance in Boost stage. Top trace: Von @2V/div, centre line is 0V; Lower traces: gate voltages on MOSFET and IGBT @10V/div; 0.5usec/div horizontal.

Fig 12 shows V1, V2, V3, and VS at turn-on. VS can be seen falling well before the other three, the voltage VE of roughly 50V can be seen, and the time T5 when V1 and V3 'jump up' can be seen. R2 and C3 were not installed when this plot was taken, thus the presence of a decaying ring after T5.

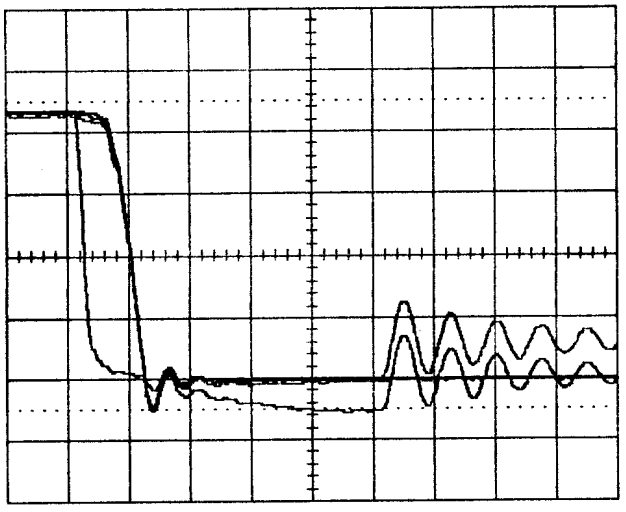

Fig 12. Observed lossless snubber operation at turn-on. 100V/div, 200nsec/div

Fig 13 shows V1, V2, V3, and VS at turn-off. The voltage VE can be seen just prior to and just after turn-off, and the action of the resetting of C1 during the 0.8*u*sec after turn-off can be seen. The voltage rises in 100nsec which is twice as slow as occurs without a snubber.

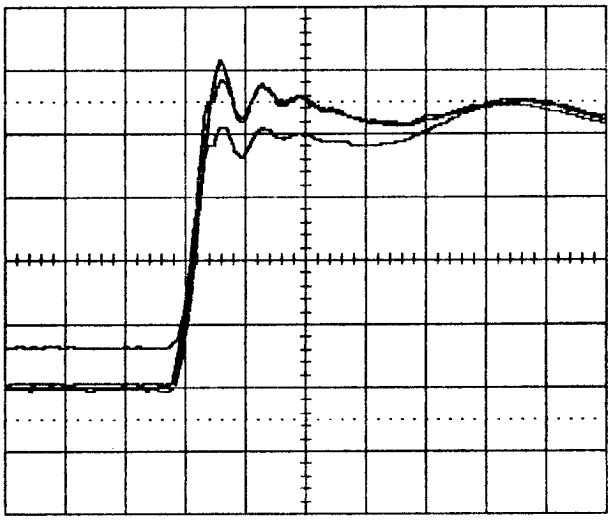

Fig 13. Observed lossless snubber operation at turn-off. 100V/div, 200nsec/div

Conclusions

A 4KW rectifier/battery charger having all the characteristics required for its use in telecommunications applications has been designed, utilising the circuits described above. The principal design objectives achieved are as follows:

- Total overall efficiency of 93%.
- Sinusoidal input current for IEC555 compliance.
- CISPR 22 Class B compliance.
- Low output noise, static and dynamic response as required for this application.
- Simplicity of power circuit for easy ability to manufacture and high reliability.

A modular approach has been implemented which enables the same basic power module complete with its control circuits to be combined with a customised front panel card. The front panel card can be designed to meet the particular requirements of any given application in terms of monitoring facilities, alarms, external controls, etc.

The power circuit can be bolted to a large sized heat sink in order to achieve 70A, 54V without fans. Alternatively a smaller heat sink may be used to achieve 50A without fans or 70A with a fan attached.

This modularity and ability to be customised makes this rectifier universally applicable to the different requirements of telecommunications authorities throughout the world.

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