New lossless clamp for single ended converters

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Abstract A clamp for single ended converters is proposed which returns energy stored in the leakage inductance of the transformer to the supply. The clamp allows minimal voltage overshoot on the switch, without employing an additional switch. The well clamped converter allows the use of lower voltage switching devices, and improves reliability of the converter.

1. Introduction

Single ended converters such as the forward, flyback, SEPIC, Cuk, and others, are often chosen for implementing simple, low cost, and low power converters. The use of only one active switch and the relatively simple control circuit required are strong reasons for this choice.

One disadvantage of single ended converters is that the leakage inductance energy in the primary circuit can, if not managed correctly, lead to voltage overshoot on the primary switching device. This in turn means that the designer must use a higher voltage rated and therefore more expensive switch. The amount of overshoot in typical configurations can exceed twice the calculated switch blocking voltage.

Besides the three well-known failure mechanisms for MOSFETs of over-dissipation, gate insulation layer breakdown and dv/dt latch-on, there exists a further failure mechanism of *avalanche overshoot* [2]. This occurs when the drain voltage rises above the normal avalanche voltage due to lack of electrons to facilitate the avalanche process. A local avalanche process discharges the distributed capacitance and the dissipation in the device in this local (tiny) area can be high enough to cause catastrophic failure. This failure mechanism seems to be entirely unrelated to the amount of energy to be clamped by the MOSFET. The risk increases when the gate voltage is driven negatively. The bottom line is that unless specific measures are taken to ensure that the MOSFET is still conducting some current when avalanche happens, it is essential that MOSFETs are prevented from avalanching, despite the manufacturers' avalanche energy rating. The conduction of current during switch-off is usually strongly avoided to reduce switching loss.

Today's designs operate at high switching frequencies to achieve small size and low cost of the passive components, so the switching device of choice is the MOSFET. The cost penalty of doubling the voltage rating of a MOSFET while maintaining the same on-resistance is about 400%, so single ended converters usually use an RCD clamp, or snub the switch so effectively that the overshoot is not excessive. Both of these measures involve significant loss.

Two frequently used alternatives for avoiding the voltage overshoot are the double ended converter, or the use of an active clamp circuit. Both of these techniques return the leakage energy to the primary energy source without incurring significant loss, and eliminate voltage overshoot on the primary. However they both involve the use of an additional active switch, and usually an additional isolated drive circuit.

A further method for reducing the voltage overshoot is the use of a low power "clamp" winding which in conjunction with a diode, as shown in Fig 1, reduces the voltage overshoot and returns most of the leakage energy to the supply. The leakage inductance between the clamp winding and the primary winding in this case limits the effectiveness of the clamp.

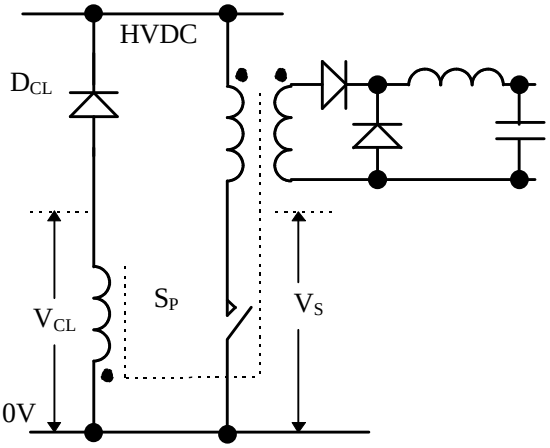

Fig 1. Forward converter with conventional clamp.

The new 'lossless' clamp circuit described in this paper virtually eliminates voltage overshoot on the switch and returns the energy to the primary circuit, without using an additional active switch and with minimal circulating energy. The additional component required compared to

the circuit of Fig 1 is one capacitor. The circuit is shown in Fig 2.

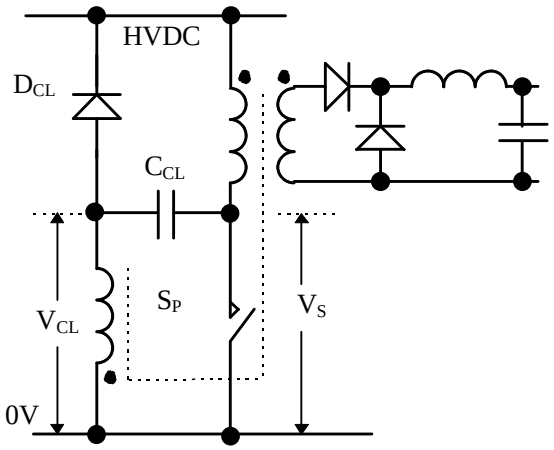

Fig 2. Forward converter with new clamp circuit.

The circuit can be applied to different topologies and these are described in the paper together with a discussion about the sizing of the components in the clamp. In particular, a forward converter is described which is used in the DC/DC converter in a 30A 48V rectifier for telecommunications applications.

2. Forward Converter Clamp Circuit

Fig 2 shows the circuit of a forward converter with the clamp circuit comprising clamp winding, clamp diode D_{CL} and clamp capacitor C_{CL}. The clamp winding has the same number of turns as the primary winding so that when V_S is 2 x HVDC, the voltage across the primary is HVDC, the voltage across the clamp winding is also HVDC so the clamp diode D_{CL} is just forward biased.

In a conventional clamp circuit which does not include C_{CL}, if the voltage V_S exceeds 2 x HVDC, then D_{CL} will conduct and current will begin flowing in the clamp winding. At some point, all the current which is forcing V_S to increase beyond 2 x HVDC will flow in D_{CL} and the voltage no longer increases.

The time taken for the current to transfer from the primary to the clamp winding, and hence the voltage overshoot beyond 2 x HVDC, is determined by the leakage inductance between the primary winding and the clamp winding.

Clamp capacitor C_{CL} has been included in order to prevent this overshoot.

The idealised waveforms for the new clamp circuit are shown in fig 3.

When starting from zero conditions with the switch S_P off, the supply voltage rises to HVDC so C_{CL} will charge to HVDC via the primary and clamp windings since they effectively form a series connection between the supply voltage and ground.

In the interval T1-T2 when S_P is on during the conduction period, V_P is near zero and since the voltage across the clamp winding is the same as that of the primary, V_{CL} is -HVDC.

When S_P switches off, the leakage and magnetic energy in the transformer charges the distributed parasitic capacitance and V_S eventually rises to 2 x HVDC. V_{CL} also increases by 2 x HVDC to HVDC. Consequently, any further increase in V_{CL} causes the clamp diode D_{CL} to be forward biased, thus effectively clamping the drain voltage of S_P via clamp capacitor C_{CL} and diode D_{CL}.

In the interval T2-T3 the load current I_O reflected in the primary winding decreases at a rate determined by the primary-secondary leakage inductance and flows through capacitor C_{CL} and diode D_{CL} to the supply. The current flow into C_{CL} during this period causes a small voltage increase across C_{CL} which depends on the value of C_{CL} and results in V_S exceeding 2HVDC by the same small amount.

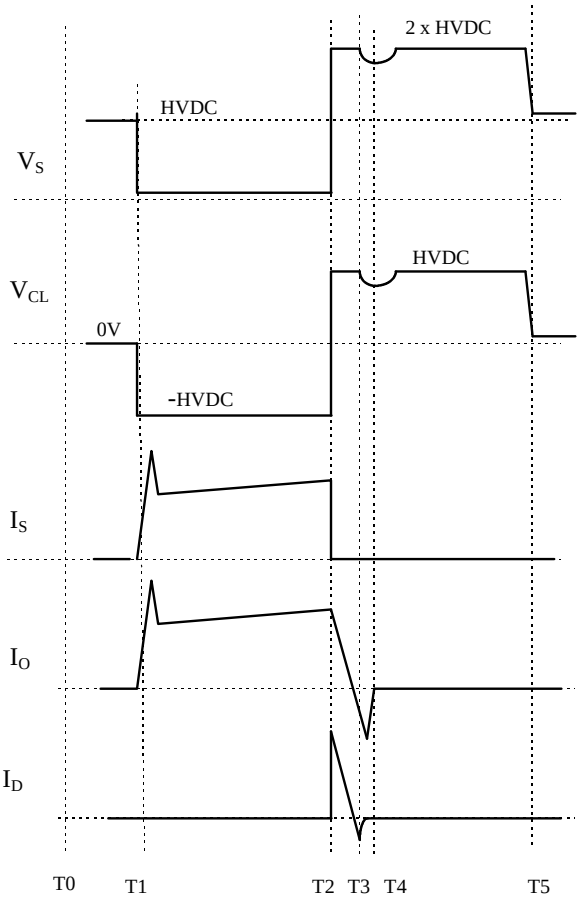

Fig 3. Idealised waveforms for lossless clamp circuit.

At T3 the primary current is negative due to the reverse recovery of the output diode and at this time D_{CL} ceases conducting after a short reverse recovery period. Since there is some output capacitance associated with the power switch voltage V_S will decrease at some rate until the reflected output diode recovery current less the primary magnetising current equals zero at T4.

In the interval T4 to T5 the decreasing but positive magnetising current will cause V_S to increase towards 2HVDC until D_{CL} once again conducts and clamps V_S to a value slightly in excess of 2HVDC. At T5 the magnetising current is zero and V_S will drop to HVDC at some rate determined by the switch capacitance.

3. Sizing of clamp capacitor C_{CL}

As mentioned above, the value of C_{CL} determines how much V_S increases above HVDC. The excess voltage dV_S is approximately given by:

$$dV_S = 0.5\ (I_O / N_{PS})(T2 - T3) / C_{CL} \qquad (1)$$

where N_{PS} is the primary to secondary turns ratio and I_O is the load current.

Assuming that the Vs rise time is small compared to the interval dT= T2-T3, dT is given by:

$$dT = L_P\ (I_O / N_{PS}) / HVDC \qquad (2)$$

where L_P is the primary-secondary leakage inductance referred to the primary winding.

Combining the two equations:

$$dV_S = 0.5\ (I_O / N_{PS})\ (L_P\ I_O/N_{PS}) / (HVDC \times C_{CL})$$

$$= 0.5\ L_P\ (I_O / N_{PS})^2 / (HVDC \times C_{CL}) \qquad (3)$$

4. Sizing of diode D_{CL}

Diode D_{CL} peak current rating must exceed I_O/N_{PS}, while its average current rating I_{AV} must be at least:

$$I_{AV} = 0.5\ (I_O / N_{PS})\ (dT/T) \qquad (4)$$

where T is the switching period. The power dissipation of the diode is determined by its forward recovery, conduction loss during the period dT and the power loss during reverse recovery.

The physical size of the diode must be carefully chosen to take into consideration the above dissipation factors. The voltage rating of the diode must of course be in excess of 2HVDC.

5. Sizing of clamp winding

There are two main current components to consider in determining the wire gauge for the clamp winding. During the conduction period T1-T2 current flows in the winding to remove charge from the clamp capacitor C_{CL}.

The second component is the magnetising current which flows during the period T3-T5.

In actual practice it is found that since it is convenient and practical to utilise one layer in the transformer for the clamp winding, the wire diameter which is used to fill the width of the single winding is such that it can very comfortably satisfy the power dissipation requirements imposed by the two current components.

6. Application of lossless clamp to other topologies

It was stated in the introduction that the clamp circuit can be applied to a wide range of single switch topologies apart from the forward converter such as flyback, SEPIC, Cuk and Zeta. Implementations of the clamp circuit applied to the above converters are shown in figs 4-8.

Applying the clamp to the flyback and ZETA converters as shown in Figs 4 and 5 holds no surprises. As in all the topologies shown, the duty cycle of the switch must be limited to 50% so that, in order to satisfy volt-time balance requirements of the transformer, it is not necessary for the off-voltage on the switch to exceed 2HVDC.

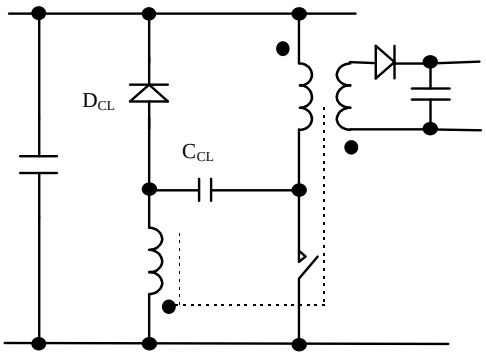

Fig 4. Flyback converter with clamp.

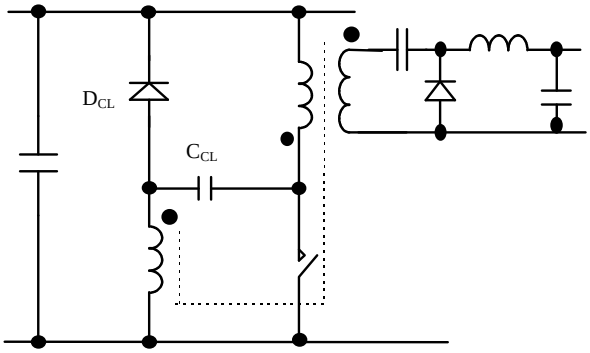

Fig 5. Zeta converter with clamp.

Of particular interest is the implementation as applied to the Cuk converter shown in Fig 6.

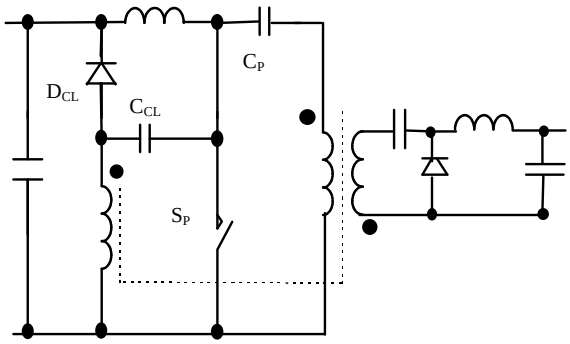

Fig 6. Cuk converter with clamp.

By inspection of Fig 6 it can be seen that the primary and clamp windings are in phase and both are joined to the power switch active terminal via capacitors C_{CL} and C_P respectively.

C_{CL} and C_P have the same average voltage across them equal to HVDC. It follows that diode D_{CL} can be moved to the position as shown in fig 7. In this instance, capacitor C_{CL} and the clamp winding can be omitted from the circuit for the same result.

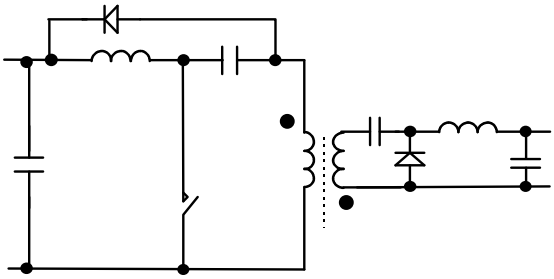

Fig 7. Cuk converter with simplified clamp.

The same argument applies in the case of the SEPIC converter as shown by the simplified clamp circuit in fig 8.

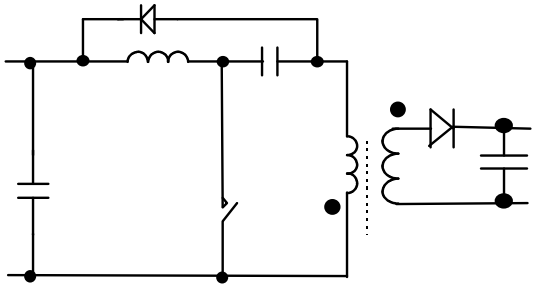

Fig 8. SEPIC converter with simplified clamp.

7. Practical application of the clamp in a 1.7 kW telecommunications rectifier

The new voltage clamp is utilised in a 48V 30A naturally cooled rectifier designed for the telecommunications industry.

The rectifier module is based on a two stage design. The first stage is a boost converter with a lossless snubber [3] and it converts the single phase input AC voltage to a regulated 420V DC supply.

The second stage is a single switch forward converter incorporating the lossless clamp as shown in fig 2, but in addition has a lossless dv/dt snubber [1] which effectively gives the stage zero voltage switching characteristics at switch-off. The transformer leakage inductance acts like a di/dt choke and gives zero current switching characteristics at switch-on. This enables operation at a frequency close to 100kHz with switching loss far below conduction loss. The forward converter stage is shown in Fig 9.

The function of the inductor L_S in series with diode D_S is to charge C_S to +HVDC when switch S_P is turned on so that when S_P is turned off, diode D_C is immediately forward biased so that primary current flows through C_S and D_C to the supply HVDC. The rate of rise of voltage on the power switch is thus controlled by C_S and can therefore be made sufficiently small that the switch-off loss is minimal.

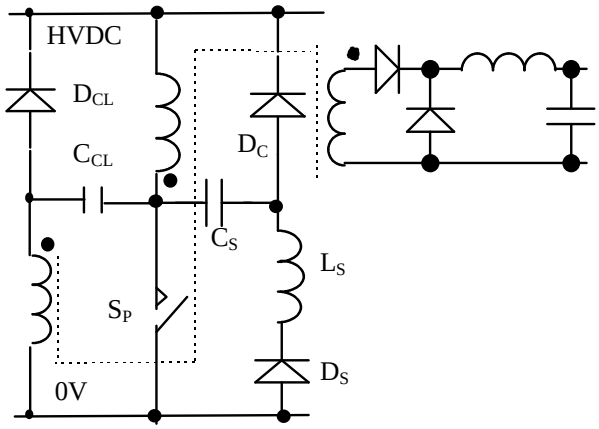

Fig 9. Forward converter with new clamp circuit.

Significantly, the charge lost by C_S during the turn-off phase is replenished in a relatively lossless way during switch-on through L_S and D_S.

At switch-on the power loss is also relatively small since the primary-secondary leakage inductance ensures a low di/dt as shown in fig 3 at T1.

The value of C_S can be chosen so that the voltage clamp circuit is virtually unnecessary. It was found however, that by having the voltage clamp circuit it is possible to choose a value of C_S which yields a higher efficiency. At the same time the clamp gives a greater certainty of voltage protection to the switch during abnormal operating conditions such as when a short circuit is applied to the output.

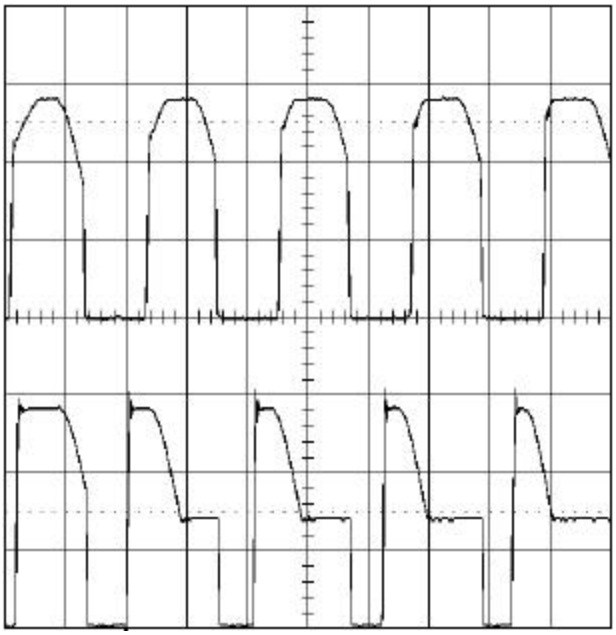

Fig 10. Drain voltage of MOSFET during application of short circuit in output. Both traces are of the same waveform, with the bottom one following the top one. Vertical scale 300V/div, horizontal scale 5us/div.

Fig 10 is the forward converter main switch drain voltage after the application of a short circuit to the output. The top trace shows the voltage increasing with each cycle and then clamping as the load current increases during the application of the short circuit. The bottom trace is the continuation of the same waveform showing very hard clamping, without which the MOSFET would have avalanched, leading to its possible failure.

Using the above circuit a very compact 1600W rectifier unit has been developed which has an overall efficiency of 91% and complies with the stringent standards required for the telecommunications applications for which it was designed.

The unit is naturally cooled and five units can fit side by side in a 19" rack magazine. A microprocessor within each unit is used to communicate alarm, control and supervisory information to a MiniCSU supervisor unit which in turn can communicate to a modem connected remote PC for central monitoring purposes.

Fig 11. 48V 30A Rectifier module.

8. Conclusion

A new, low component count, lossless clamp circuit has been described which is very effective in preventing overvoltage spikes in a number of single switch converters. This offers the advantage of enabling the use of lower $R_{DS(ON)}$ rated MOSFETs than would otherwise be possible and consequently saves on component costs while at the same time maximising the efficiency obtained as well as the reliability of the circuit.

References

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[2] C. J. Hammerton, "*Avalanche Overshoot Poses a Hazard for MOSFETs"*, Power Conversion & Intelligent Motion January 1996, pp 52-57

[3] N. Machin & T. Vescovi, "*Very High Efficiency Techniques and their Selective Application to the Design of a 70A Rectifier*", INTELEC Proceedings 1993.